长鑫集电（北京）存储技术有限公司
参与高等职业教育人才培养年度报告（2023）

一、公司情况介绍

长鑫存储的事业开始于 2016 年，专业从事动态随机存取存储芯片（DRAM）的研发、生产和销售，目前 12 英寸晶圆厂已建成投产。DRAM 产品广泛应用于移动终端、电脑、服务器、虚拟现实和物联网等领域，市场需求巨大并持续增长。公司自成立以来，以技术为核心，加强管理体系的建设。在奇梦达技术的基础上，公司利用专用研发线快速迭代研发，同时结合当前先进设备大幅度改进工艺，开发出独有的技术体系，成为奇梦达技术的继承者和发扬者。长鑫存储将凭借值得信赖的产品和服务满足不断增长的市场需求，致力于成为技术领先与商业成功的半导体存储芯片公司，以存储科技赋能信息社会，改善人类生活。

长鑫存储子公司长鑫集电（北京）存储技术有限公司位于北京经开区，目前注册资本 448.1 亿元，公司主要负责建设运营北京 DRAM 存储器示范线项目，旨在快速落地先进 DRAM 工艺。

CONFIDENTIAL

二、企业资源投入

为满足企业人才需求，长鑫集电与北京信息职业技术学院开展校企合作，坚持“优势互补、资源共享、互利共赢”的原则，建立订单培养机制，学校组织、推荐学生报名参加企业的订单培养项目遴选；企业妥善安排学生在公司进行岗位综合素质训练和专业知识及技能学习，并向学校出具学生在实习期间的企业实践成绩和实习

鉴定；双方共同制定联合培养方案。

三、产教融合情况介绍

长鑫集电一直以来积极协调优质高校资源，在充分发挥产业链上下游协同作用的基础上，打通了人才培养通道，形成了校企联合培养人才的创新模式。

长鑫集电积极与北京市属高校、高职加强人才联合培养。与学校共同研讨集成电路人才需求及能力建设需求，以用促学，自 2021 年至今已招聘北京信息职业技术学院学生 70 人，分布在设备技术员、厂务技术员、IT 技术员、生产技术员等重要岗位，其中不少优秀毕业生已成为企业骨干型人才。

四、学生培养

企业为学生提供顶岗实习机会，将半导体生产知识及生产安全的知识和意识提前导入，对学生今后进入产业打下良好基础，通过生产性实训，使学生全面了解企业运营，在真实的工作环境下，体会理论与实践的有机结合，在感性认识和理性认识上产生一个飞跃。最关键是让学生了解企业文化，感受企业管理制度，明确自己职业生涯的目标。通过企业导师的指导，学生养成了良好的职业素质，包括职业道德、团队合作精神、解决问题的能力等。获得了良好的社会效益：校企合作订单班的学生在实习或毕业后得到了企业的信任和支持，为企业创造了良好的社会效益。

五、总结

校企合作订单班是培养具有实践能力和创新精神人才的重要途

CONFIDENTIAL

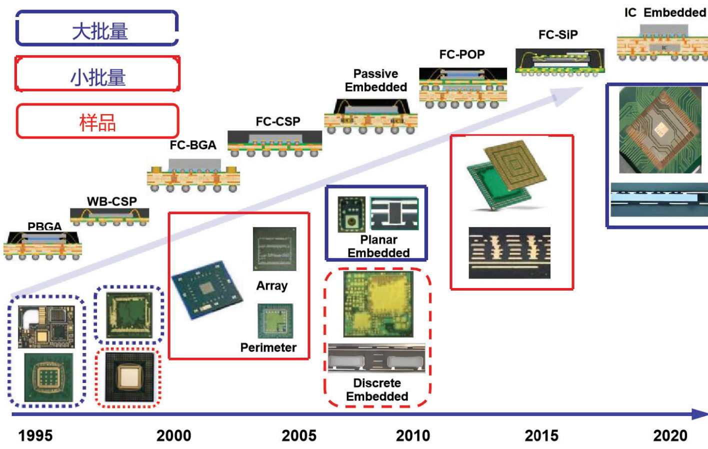
径。通过校企合作，订单班学生获得了实践机会，提高了职业技能和就业竞争力。同时，校企合作订单班也为企业提供了人才储备和品牌效应，有助于提升企业的市场竞争力。未来，校企双方需要进一步加强合作，共同提高人才培养质量，为学生提供更多的实习和就业机会。品牌效应，有助于提升企业的市场竞争力。未来，校企双方需要进一步加强合作，共同提高人才培养质量，为学生提供更多的实习和就业机会。

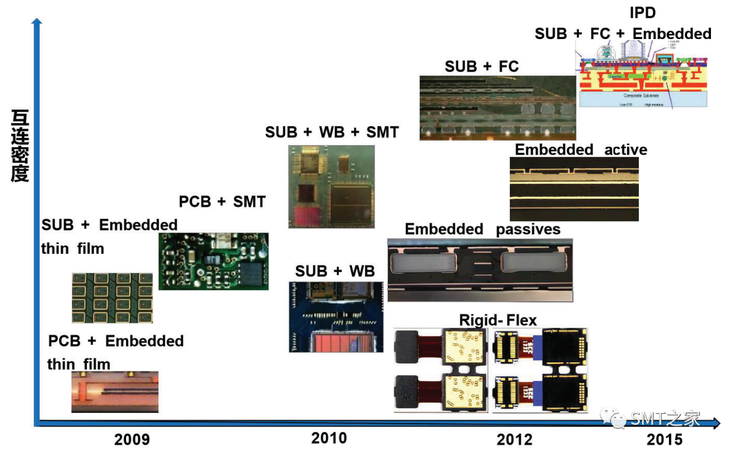
长鑫集电（北京）存储技术有限公司

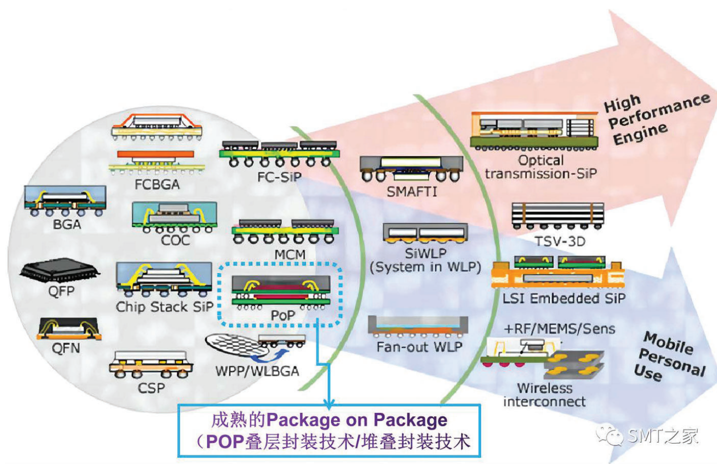
2023 年 12 月 29 日

CONFIDENTIAL

封装与高密度基板行业发展趋势







先 进 封 装 技 术

Advanced Packaging Tech

先 进 封 装 技 术

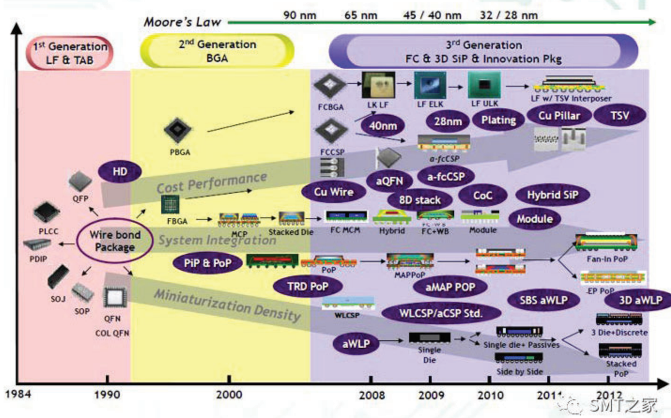
SMT之家

Outline 概述

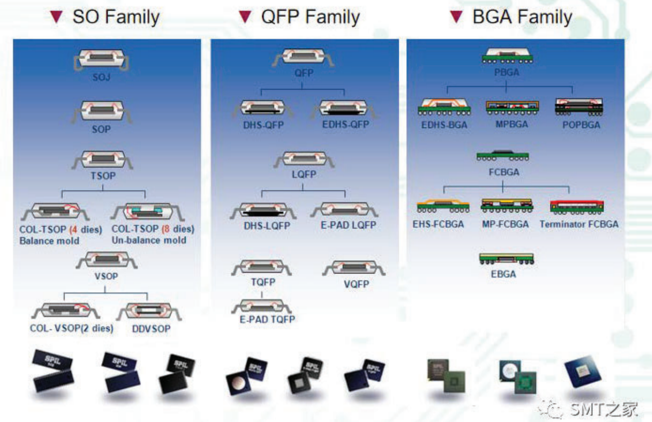
- Package Development Trend
  封装发展趋势
- 3D Package
  3D封装
- WLCSP & Flip Chip Package
  晶圆级芯片封装和倒装芯片封装

SMT之家

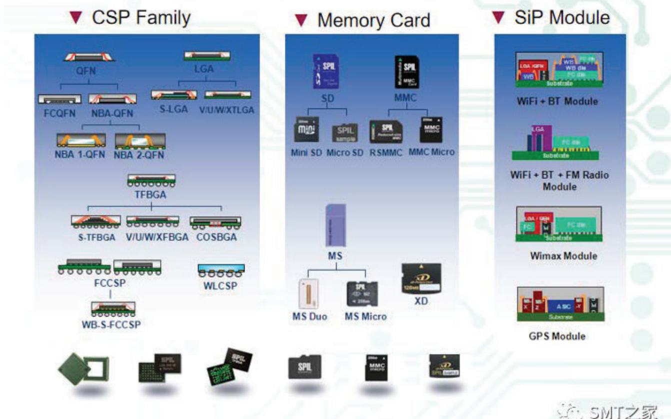
Package Development Trend 封装发展趋势



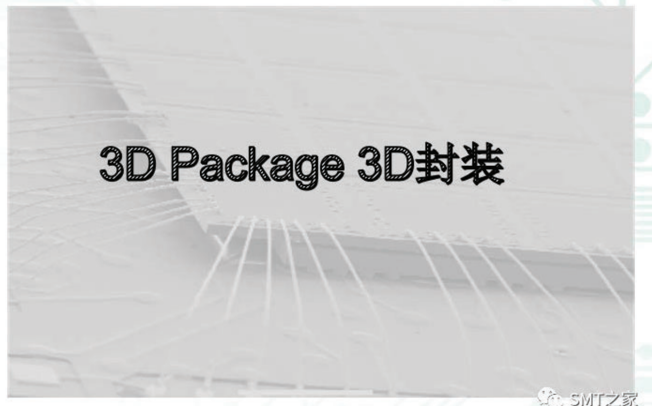
Package Development Trend 封装发展趋势



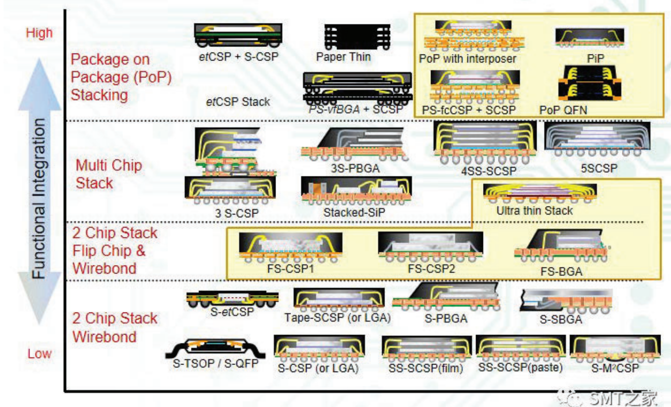
Package Development Trend 封装发展趋势



3D Package 3D封装



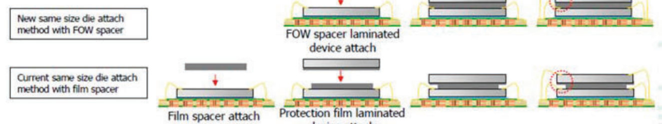
3D Package Introduction 3D封装介绍

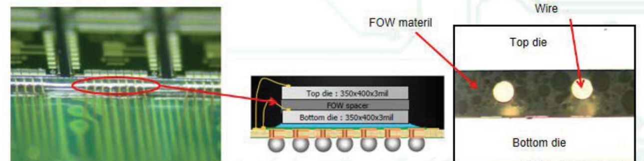


Stacked Die 堆叠Die

Process flow of FOW and Film Spacer

- If FOW spacer is applied to same size die attach, the film spacer cut & place machine(module) is not required, UPH can be increased, and wire bond ability for top die will be improved by supported wire bonding area(no die overhang).





TSV 硅通孔

▼ TSV (Through Silicon Via)

A through-silicon via (TSV) is a vertical electrical connection (via) passing completely through a silicon wafer or die. TSV technology is important in creating 3D packages and 3D integrated circuits.

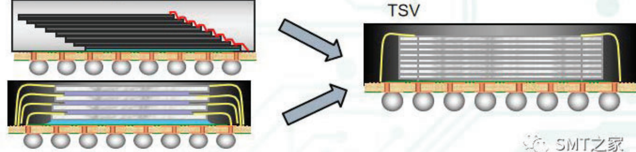
A 3D package (System in Package, Chip Stack MCM, etc.) contains two or more chips (integrated circuits) stacked vertically so that they occupy less space.

In most 3D packages, the stacked chips are wired together along their edges. This edge wiring slightly increases the length and width of the package and usually requires an extra "interposer" layer between the chips.

In some new 3D packages, through-silicon via replace edge wiring by creating vertical connections through the body of the chips. The resulting package has no added length or thickness.

Wire Bonding Stacked Die

TSV



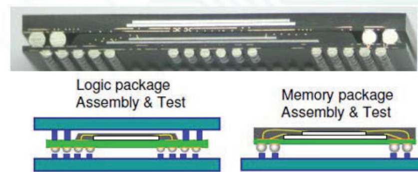
SMT之家

PoP 堆叠封装

▼ What's PoP?

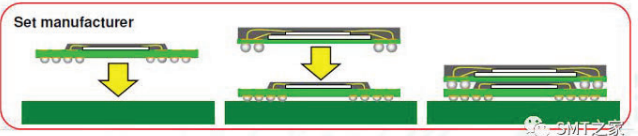
▲ PoP is Package on Package

▲ Top and bottom packages are tested separately by device manufacturer or subcon.



Logic package Assembly & Test

Memory package Assembly & Test

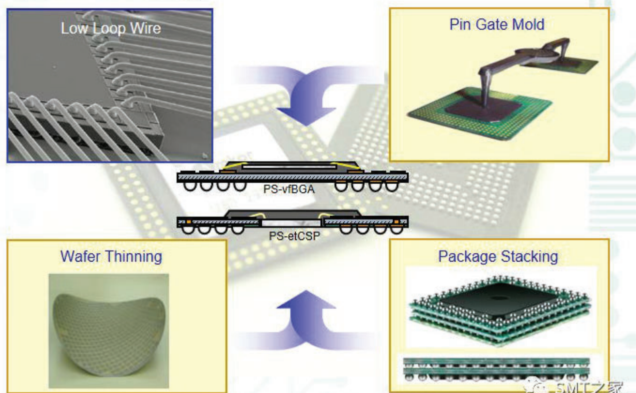


Set manufacturer

SMT之家

PoP 堆叠封装

▼ PoP Core Technology



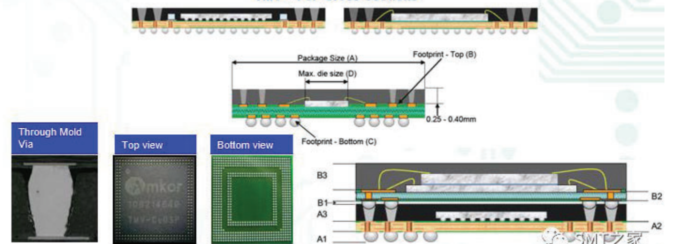
SMT之家

PoP 堆叠封装

▼ Amkor's TMV™ PoP

- ▼ Allows for warpage reduction by utilizing fully-molded structure
  - ▲ More compatible with substrate thickness reduction
- ▼ Provides fine pitch top package interface with thru mold via
- ▼ Improved board level reliability
- ▼ Larger die size / package size ratio
- ▼ Compatible with flip chip, wire bond, or stacked die configurations
- ▼ Cost effective compared to alternative next generation solutions

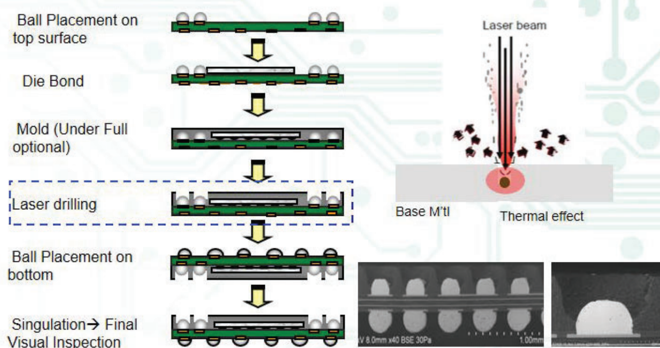
TMV™ PoP Cross Sections



SMT之家

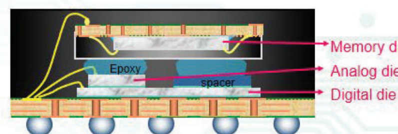
PoP 堆叠封装

▼ Process Flow of TMV PoP



SMT之家

PIP



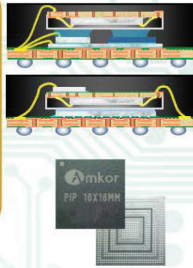
- ☐ Digital(Btm die) + Analog(Middle die) + Memory(Top pkg)
- ☐ Potable Digital Gadget
  - ■ Cellular Phone, Digital Still Camera, Potable Game Unit

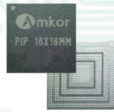
SMT之家

PIP

▼ Why PiP?

✓Easy system integration 易于系统集成
✓Flexible memory configuration 灵活的内存配置
✓100% memory KGD 100 %KGD内存
✓Thinner package than POP 封装比 POP更薄
✓High IO interconnection than POP IO互连比 POP高
✓Small footprint in CSP format CSP 格式占用空间小





It has standard ball size and pitch
球的大小和间距有标准

Constructed with: 有以下构造：
- Film Adhesive die attach 薄膜粘合模具连接
- Epoxy paste for Top PKG 顶部 PKG 用环氧浆
- Au wire bonding for interconnection 使用金线键合互连
- Mold encapsulation 模具封装

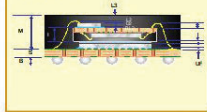
SMT之家

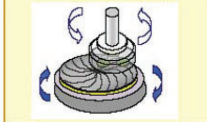
PIP

▼ PiP Core Technology

Optimized Package Design
封装设计优化

Material for High Reliability Based on Low Warpage
基于低翘曲的高可靠性材料





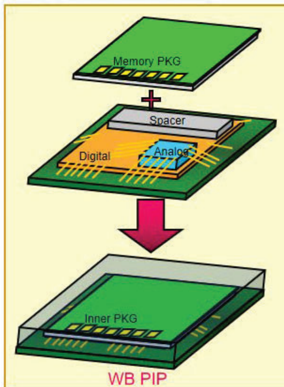
Wafer Thinning硅片减薄

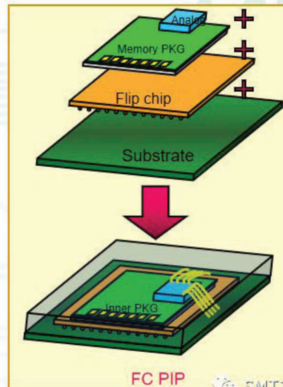
Fine Process Control
精细过程控制
- Top Package Attach
- Die Attach
- etc

SMT之家

PIP

▼ PiP – W/B PiP and FC PiP





SMT之家

WLCSP & Flip Chip Package
晶圆级芯片封装&倒装芯片封装

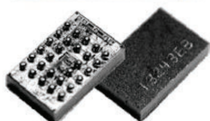
SMT之家

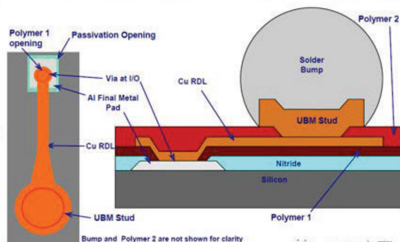
WLCSP 晶圆级芯片级封装

☐ What is WLCSP?

WLCSP(Wafer Level Chip Scale Packaging), is not same as traditional packaging method (dicing→ packaging→ testing, package size is at least 20% increased compared to die size).

WLCSP is packaging and testing on wafer base, and dicing later. So the package size is exactly same as bare die size. WLCSP can make ultra small package size, and high electrical performance because of the short interconnection.





SMT之家

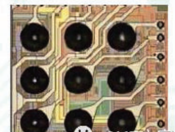
WLCSP 晶圆级芯片级封装

☐ Why WLCSP?

- Smallest package size: WLCSP have the smallest package size against die size. So it has widely use in mobile devices.
- High electrical performance: because of the short and thick trace routing in RDL, it gives high SI and reduced IR drop.
- High thermal performance: since there is no plastic or ceramic molding cap, heat from die can easily spread out.
- Low cost: no need substrate, only one time testing.

☐ WLCSP's disadvantage

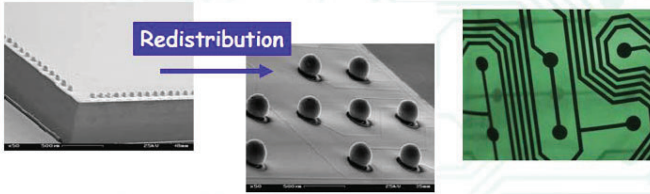
- Because of the die size and pin pitch limitation, IO quantity is limited (usually less than 50pins).
- Because of the RDL, stagger IO is not allowed for WLCSP.



SMT之家

RDL

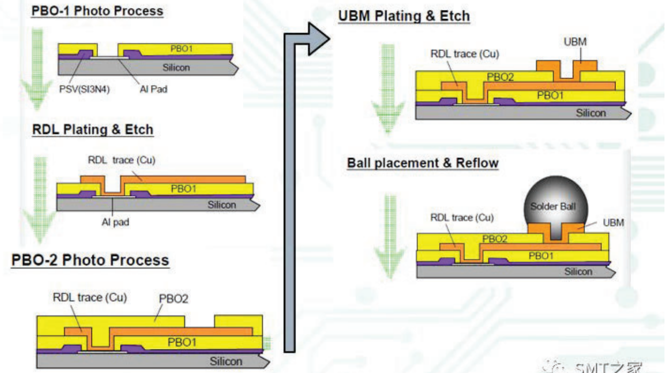
- RDL: Redistribution Layer
  - A redistribution layer (RDL) is a set of traces built up on a wafer's active surface to re-route the bond pads. This is done to increase the spacing between each interconnection(bump).



SMT之家

WLCSP

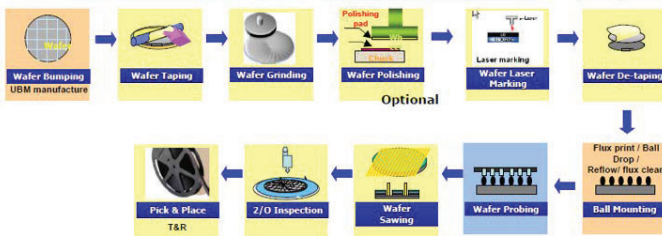
- Process Flow of WLCSP



SMT之家

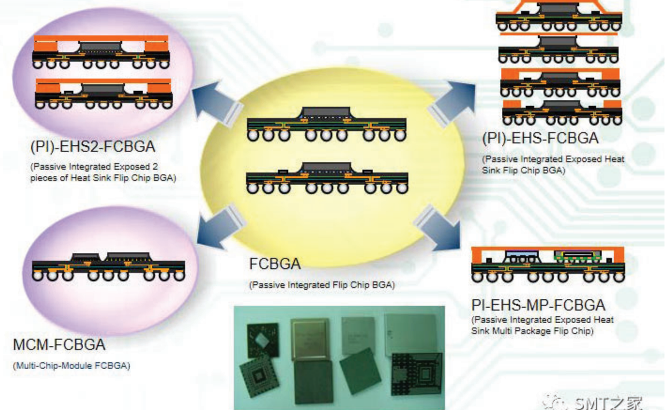
WLCSP

- Process Flow of WLCSP



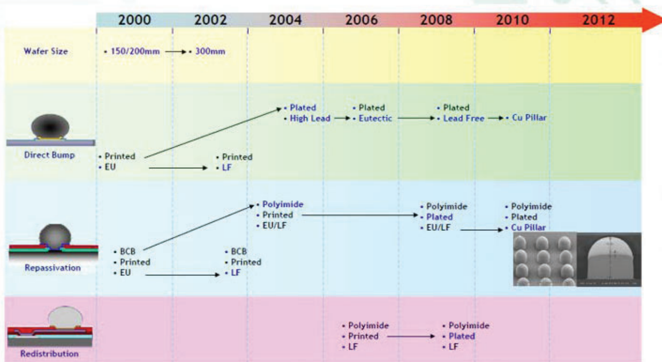
SMT之家

Flip Chip Package 倒装芯片封装



SMT之家

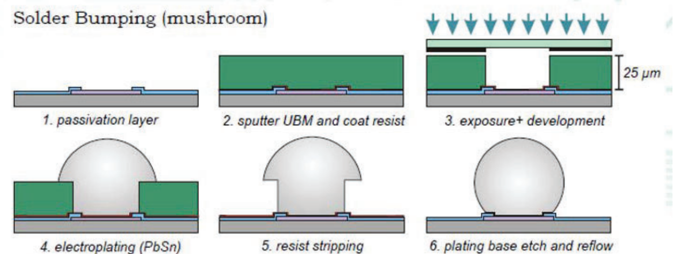
Bump 凸点



SMT之家

Bump Development 凸点开发

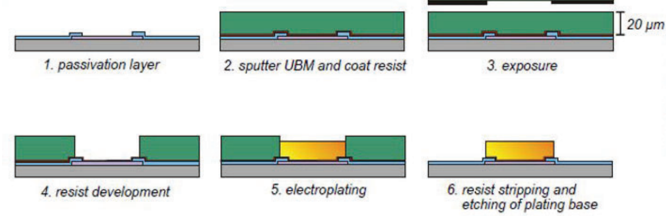
Solder Bumping (mushroom)



SMT之家

Bump Development 凸点开发

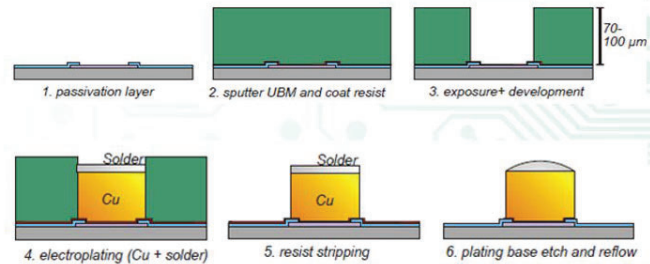
Gold Bumping



SMT之家

Bump Development 凸点开发

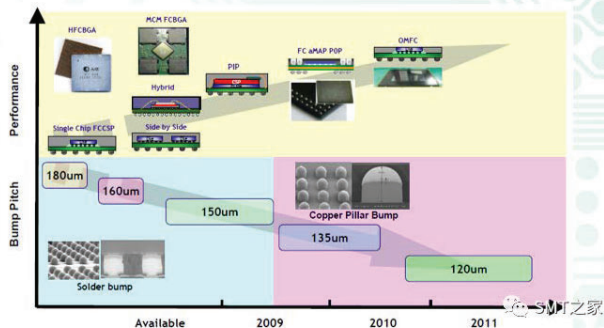
Copper Posts



SMT之家

C4 Flip Chip C4倒装芯片

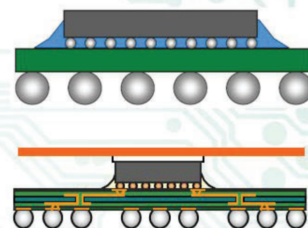
- What's C4 Flip Chip?
  - C4 is: Controlled Collapsed Chip Connection 受控折叠芯片连接
  - Chip is connected to substrate by RDL and Bump 芯片通过RDL和凸点连接到基板
  - Bump material type: solder, gold 凸点材料类型：焊料、金线



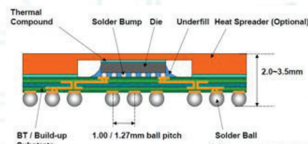
SMT之家

C4 Flip Chip BGA C4倒装BGA芯片

- Main Features
  - Ball Pitch:0.4mm - 1.27mm
  - Package size: up to 55mmx55mm
  - Substrate layer: 4-16 Layers
  - Ball Count: up to 2912
  - Target Market: CPU、FPGA、Processor、Chipset 、Memory、Router、 Switches、and DSP etc.



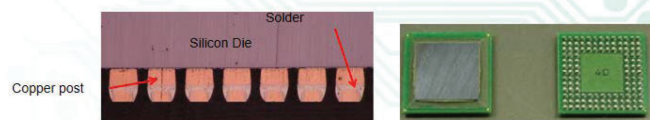
- Main Benefits
  - Reduced Signal Inductance
  - Reduced Power/Ground Inductance
  - Higher Signal Density
  - Die Shrink & Reduced Package Footprint
  - High Speed and High thermal support



SMT之家

C2 Flip Chip C2倒装芯片

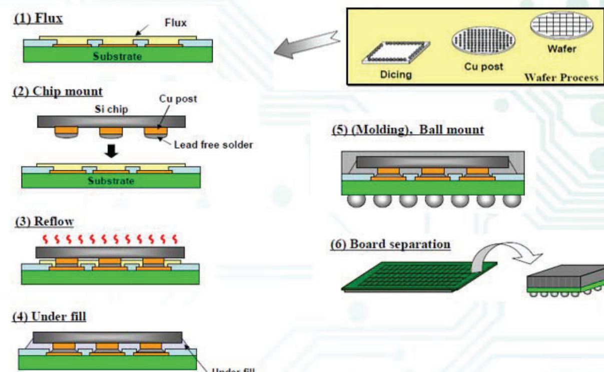
- What's C2 Flip Chip?
  - C2 is: Chip Connection
  - Chip is connected to substrate by copper post
  - Bump material type: copper post with solder plating



SMT之家

C2 Flip Chip C2倒装芯片

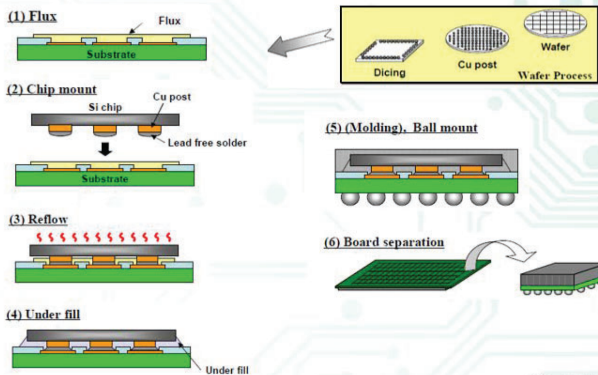
- Process Flow of C2



SMT之家

C2 Flip Chip C2倒装芯片

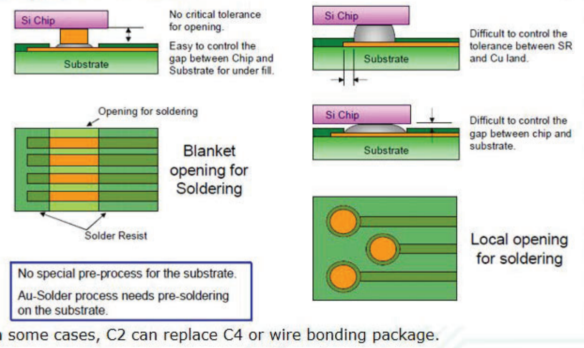
▼ Process Flow of C2



SMT之家

C2 Flip Chip C2倒装芯片

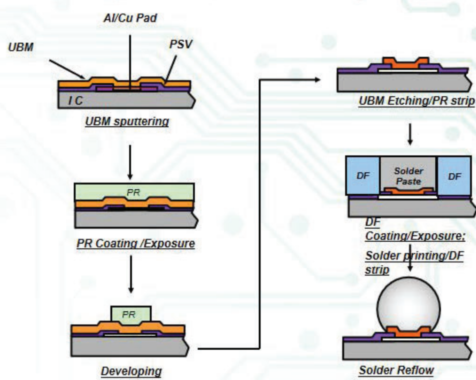
▼ Comparison: C2 Vs C4



In some cases, C2 can replace C4 or wire bonding package.

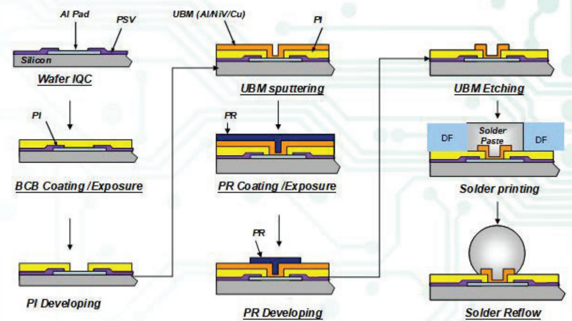
SMT之家

Bumping process flow-FOC Printing 凸版印刷工艺流程



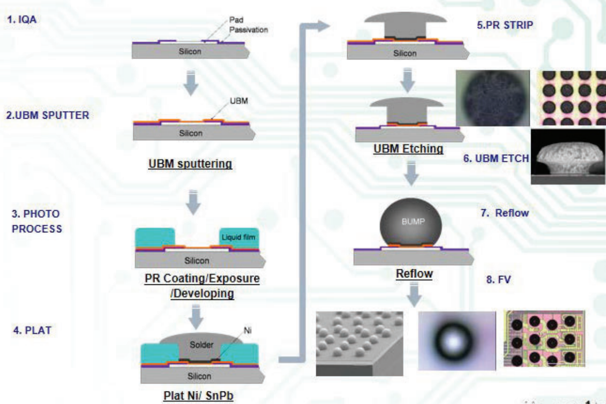
SMT之家

REPSV Printing Bump Process Flow 印刷凸点工艺流程



SMT之家

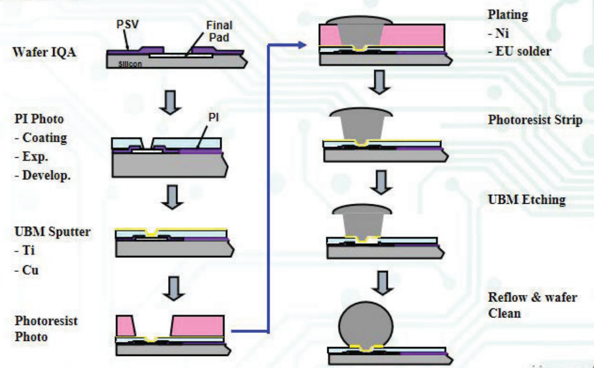
Plating Process – FOC Flow 电镀工艺- FOC 流程



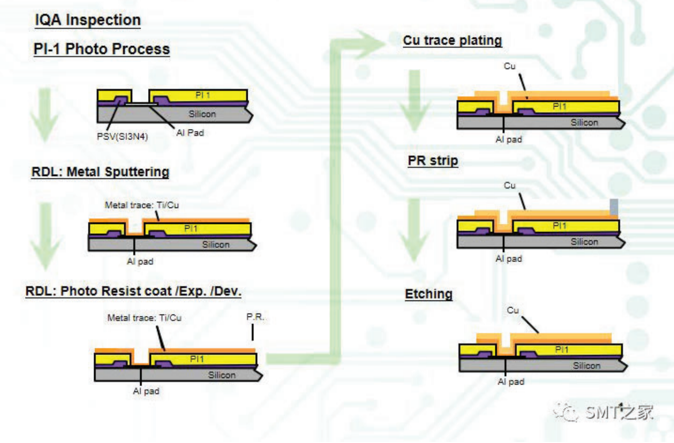
SMT之家

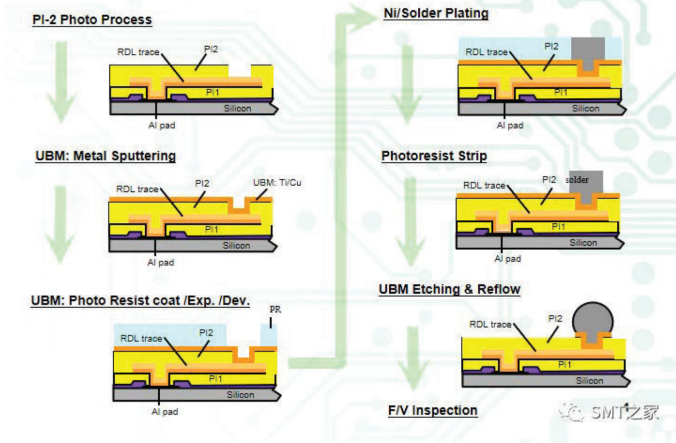
REPSV Plating Process Flow 电镀工艺流程

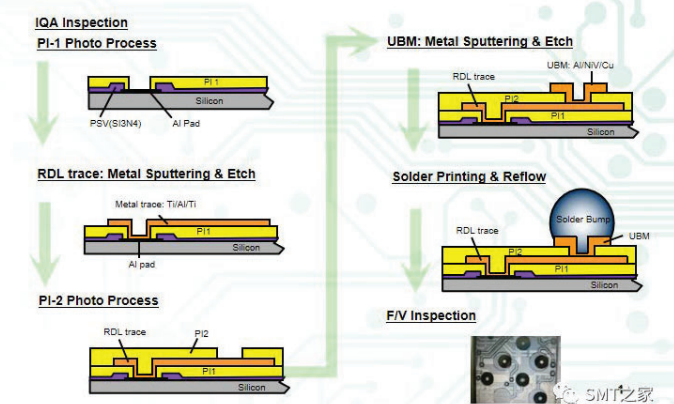
PI RePSV

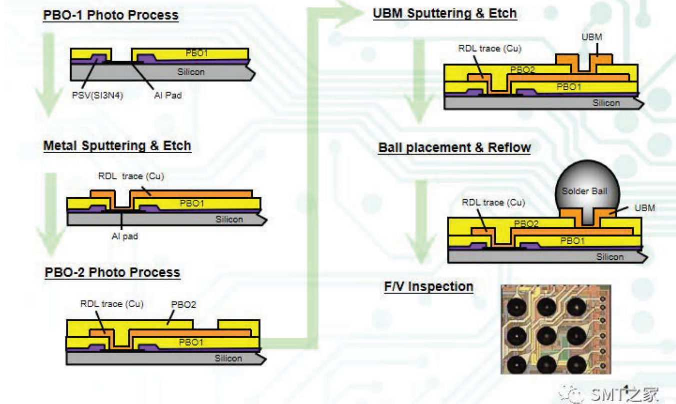


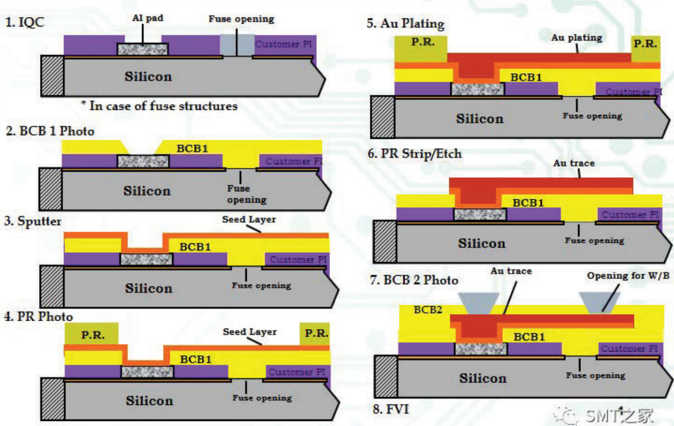
SMT之家

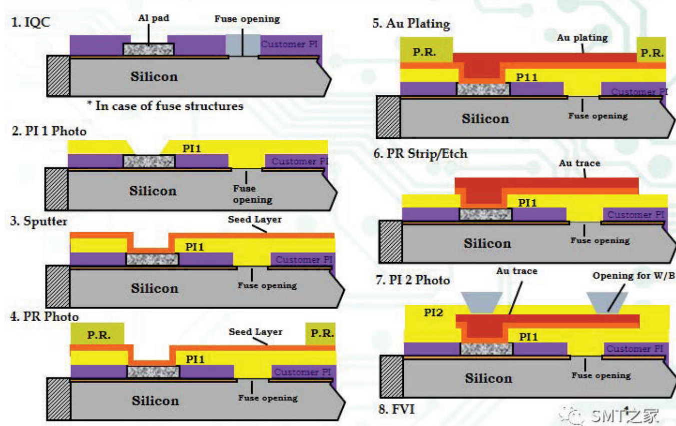

Plated RDL Process Flow(1/2) 电镀 RDL 工艺流程（1/2）
IQA Inspection
PI-1 Photo Process
PI1
Silicon
PSV(SI3N4)
Al Pad
RDL: Metal Sputtering
Metal trace: Ti/Cu
Al pad
RDL: Photo Resist coat /Exp. /Dev.
P.R.
Cu trace plating
Cu
PR strip
Etching


Plated RDL Process Flow(2/2) 电镀RDL工艺流程（2/2）
PI-2 Photo Process
RDL trace
PI2
PI1
Silicon
Al pad
UBM: Metal Sputtering
UBM: Ti/Cu
UBM: Photo Resist coat /Exp. /Dev.
PR
Ni/Solder Plating
Photoresist Strip
solder
UBM Etching & Reflow
F/V Inspection

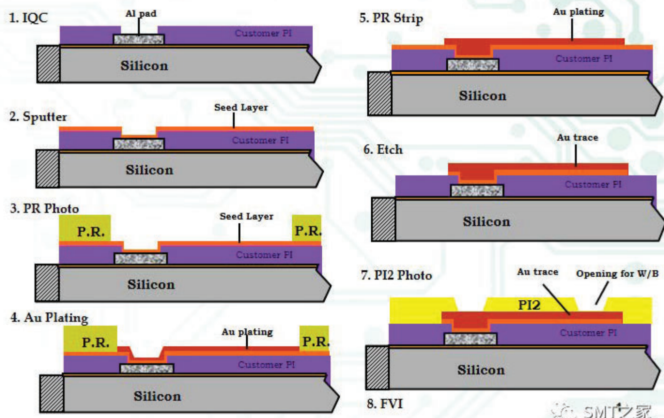

Printed RDL Process Flow 印刷RDL工艺流程
IQA Inspection
PI-1 Photo Process
PI 1
Silicon
PSV(SI3N4)
Al Pad
RDL trace: Metal Sputtering & Etch
Metal trace: Ti/Al/Ti
Al pad
PI-2 Photo Process
RDL trace
PI2
UBM: Metal Sputtering & Etch
UBM: Al/NiV/Cu
Solder Printing & Reflow
Solder Bump
UBM
F/V Inspection


BP-WLCSP Process Flow BP-晶圆级芯片封装工艺流程
PBO-1 Photo Process
PBO1
Silicon
PSV(SI3N4)
Al Pad
Metal Sputtering & Etch
RDL trace (Cu)
Al pad
PBO-2 Photo Process
PBO2
UBM Sputtering & Etch
UBM
Ball placement & Reflow
Solder Ball
F/V Inspection


Au RDL Process Flow (BCB1+Au Trace+BCB2)(for DRAM device)
1. IQC
Al pad
Fuse opening
Customer PI
Silicon
* In case of fuse structures
2. BCB 1 Photo
BCB1
3. Sputter
Seed Layer
4. PR Photo
P.R.
5. Au Plating
Au plating
6. PR Strip/Etch
Au trace
7. BCB 2 Photo
Opening for W/B
BCB2
8. FVI


Au RDL Process Flow (PI1+Au Trace+PI2)(for Flash or Controller device)
1. IQC
Al pad
Fuse opening
Customer PI
Silicon
* In case of fuse structures
2. PI 1 Photo
PI1
3. Sputter
Seed Layer
4. PR Photo
P.R.
5. Au Plating
Au plating
6. PR Strip/Etch
Au trace
7. PI 2 Photo
Opening for W/B
PI2
8. FVI

Au RDL Process Flow (Au Trace + PI)(for Flash device)



WLCSP Backend Process Flow

WLCSP Backend Process Flow

WF Mount & De-Tapping